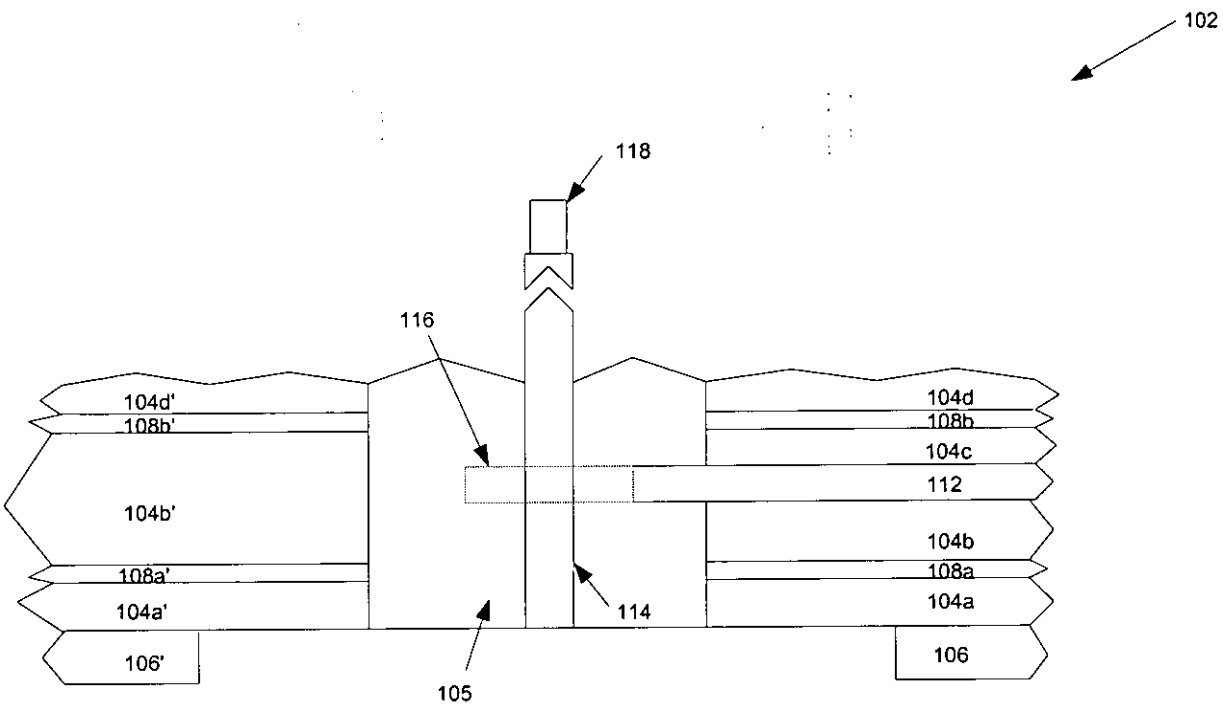
102
118
116
104d'
108b'
104b'
108a'
104a'
106'
105
114
104d
108b
104c
112
104b
108a
104a
106

FIG. 1a

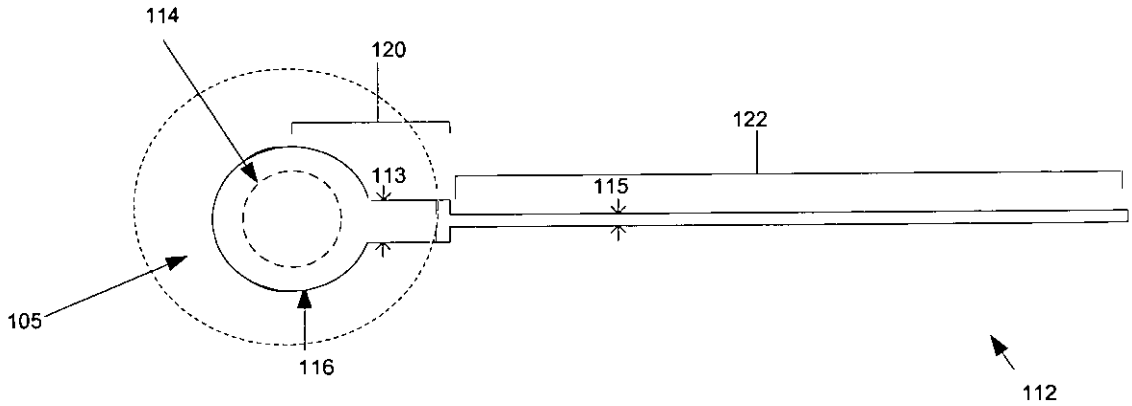

FIG. 1b

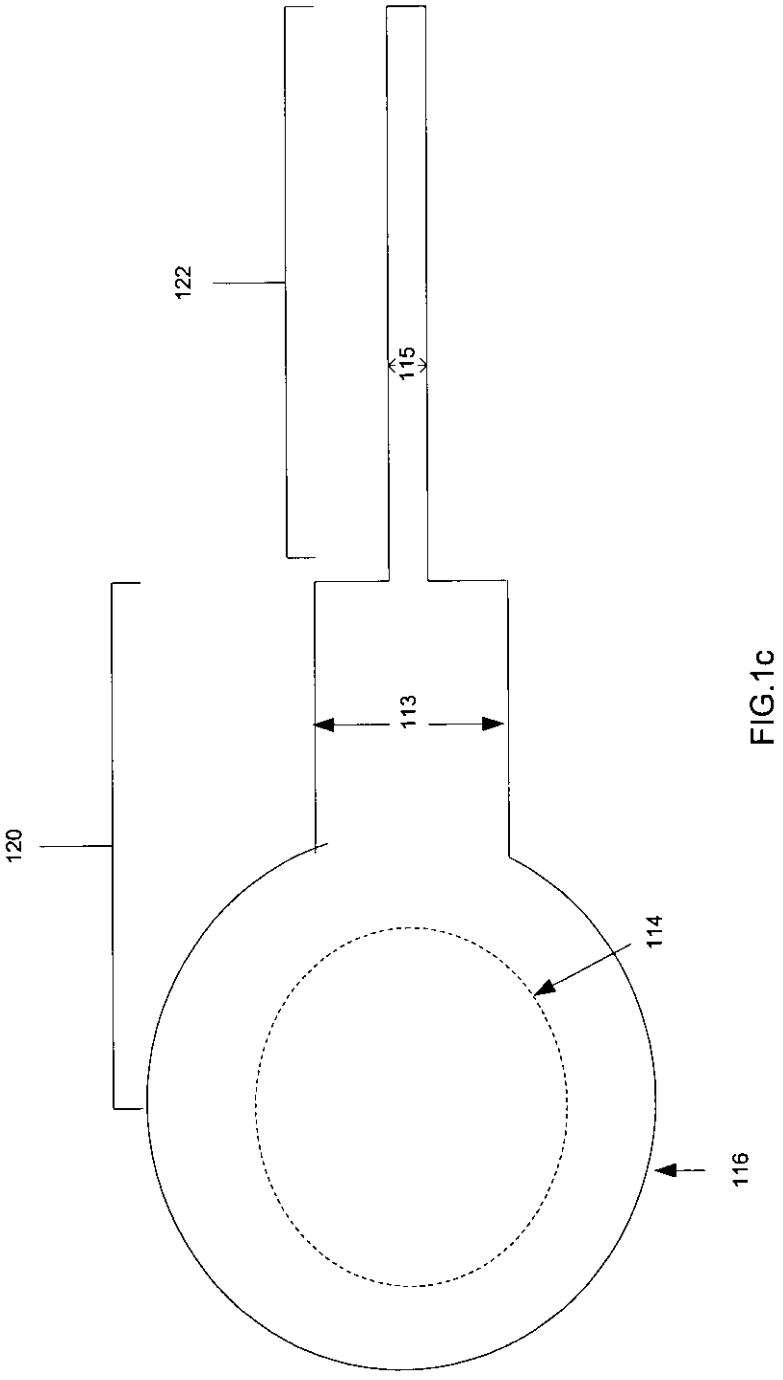

FIG.1c

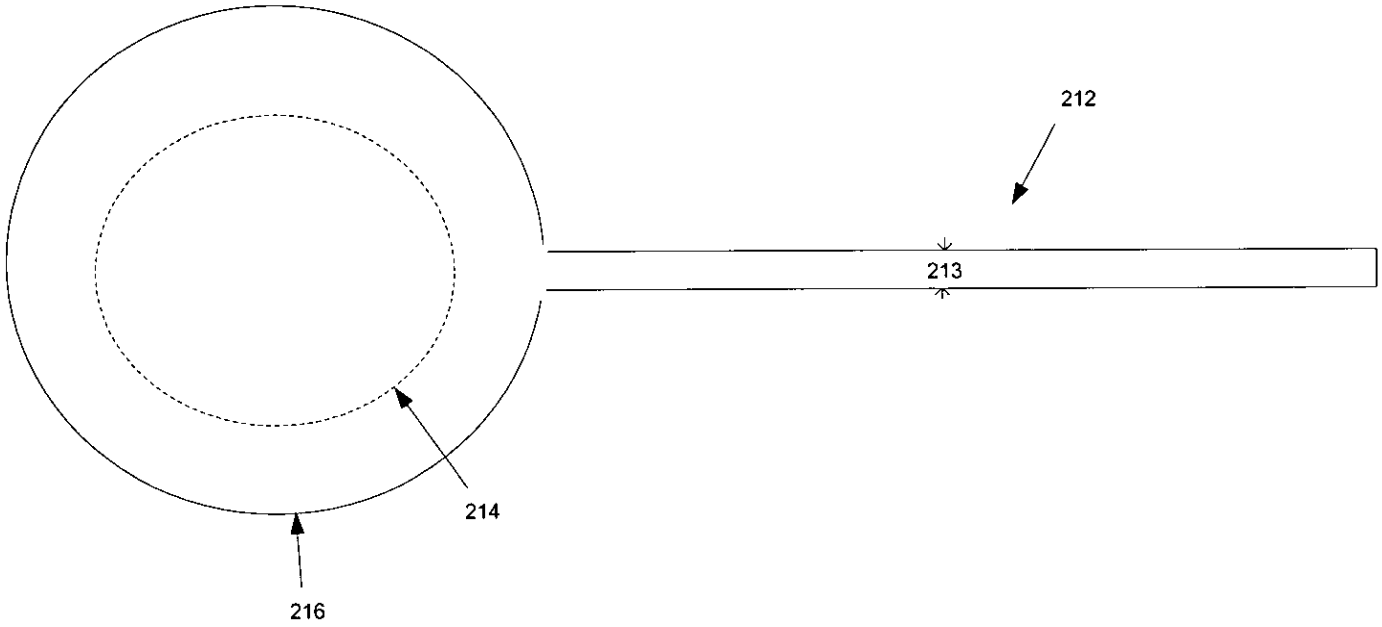

FIG.2a

(Prior Art)

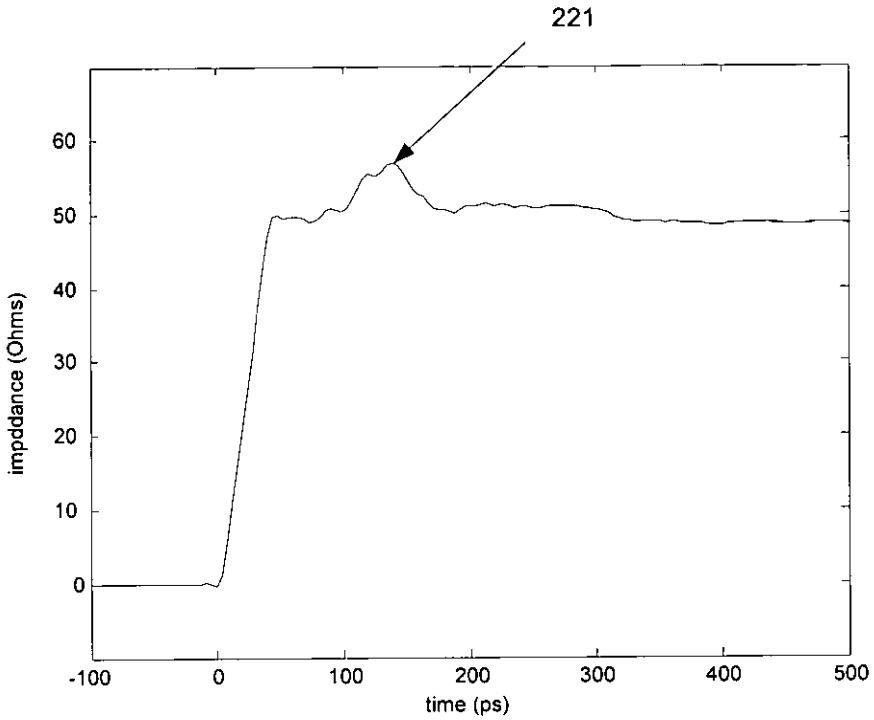

FIG. 2b
(Prior Art)

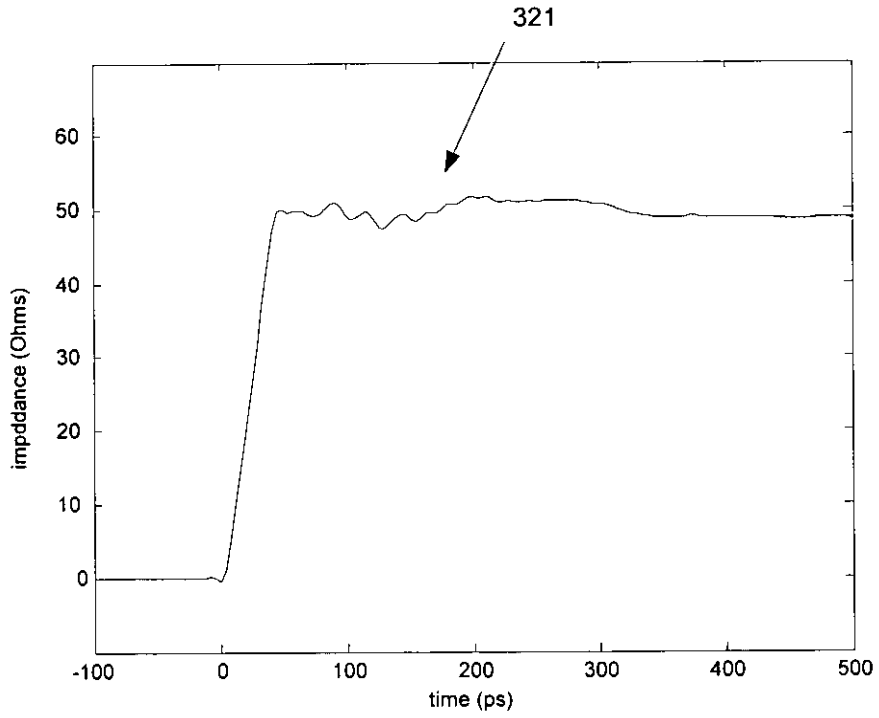

FIG. 3

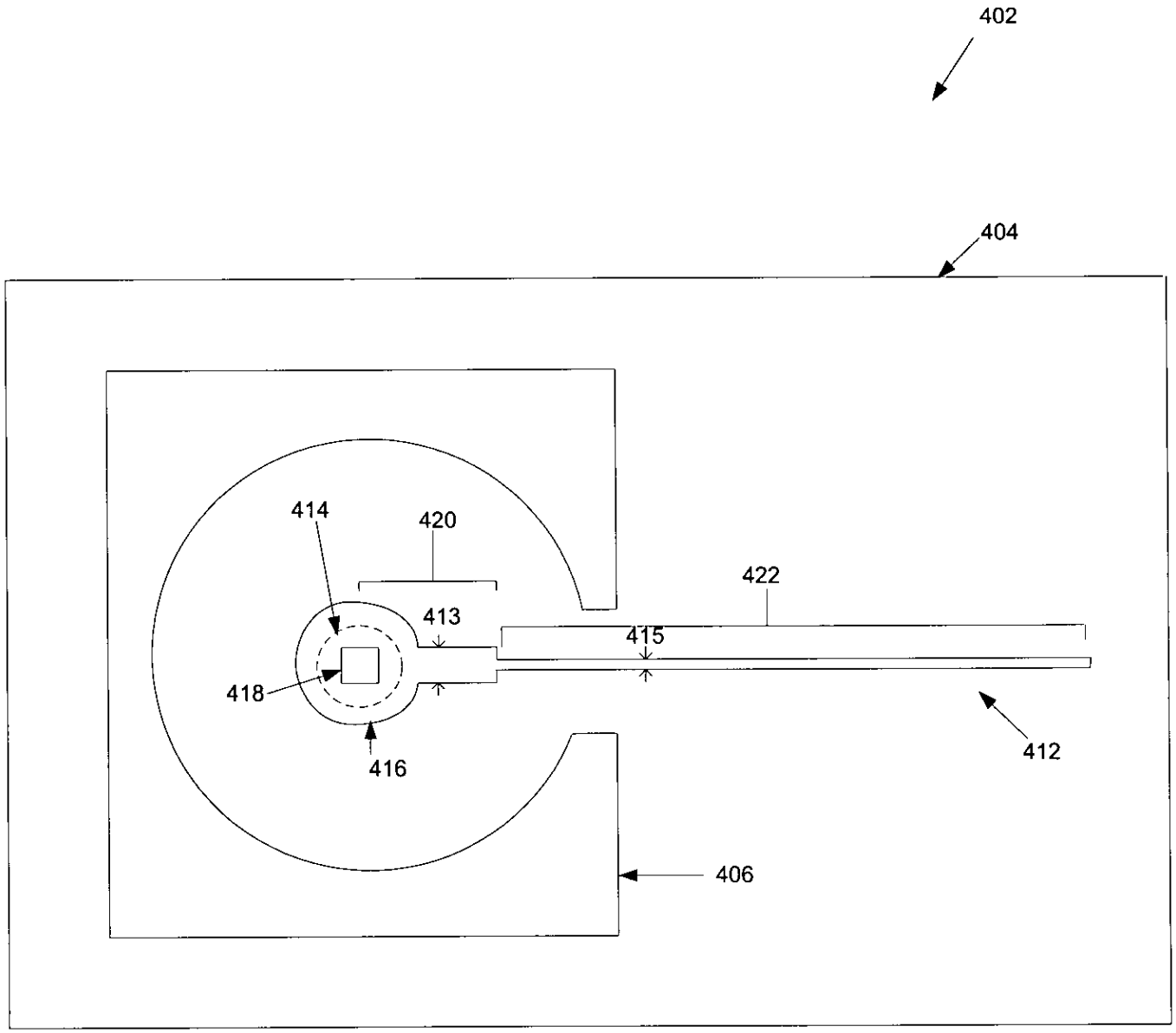

FIG. 4a

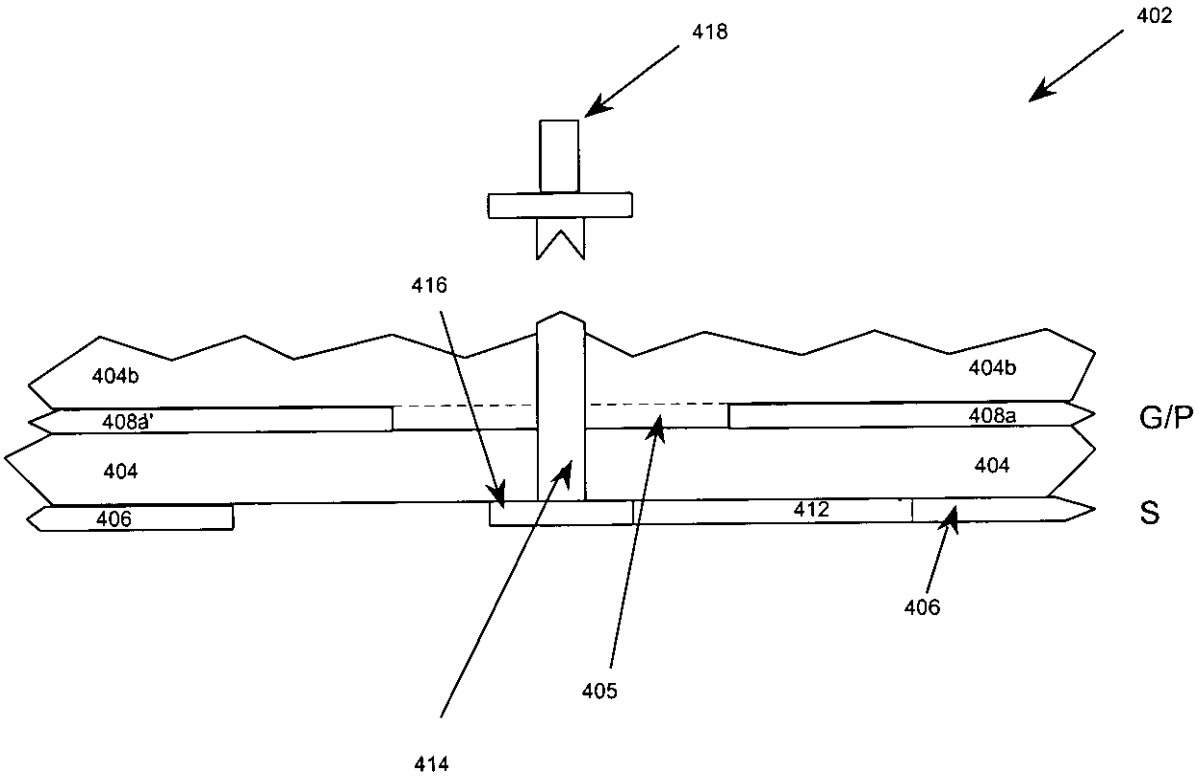

FIG. 4b

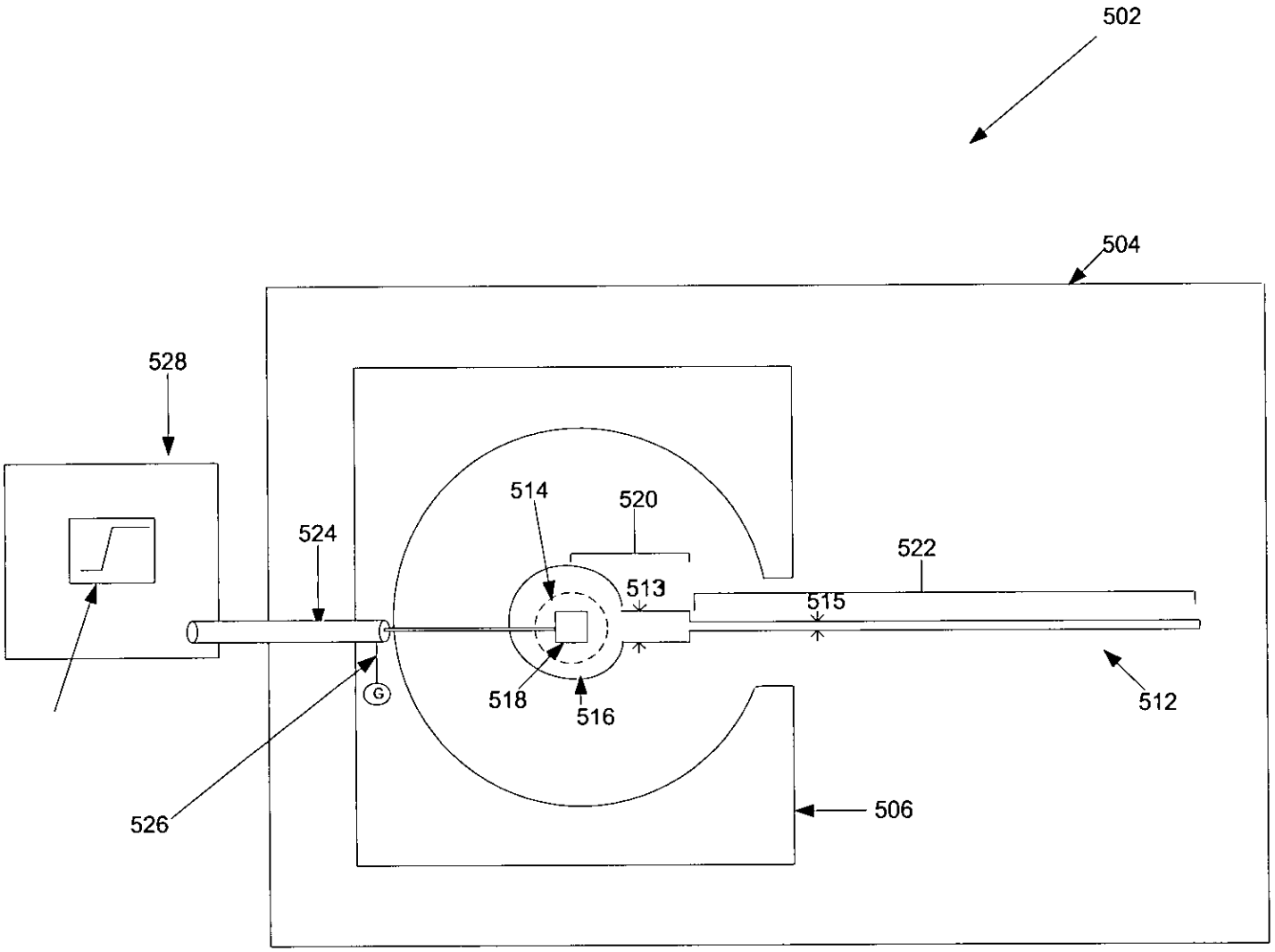

FIG. 5

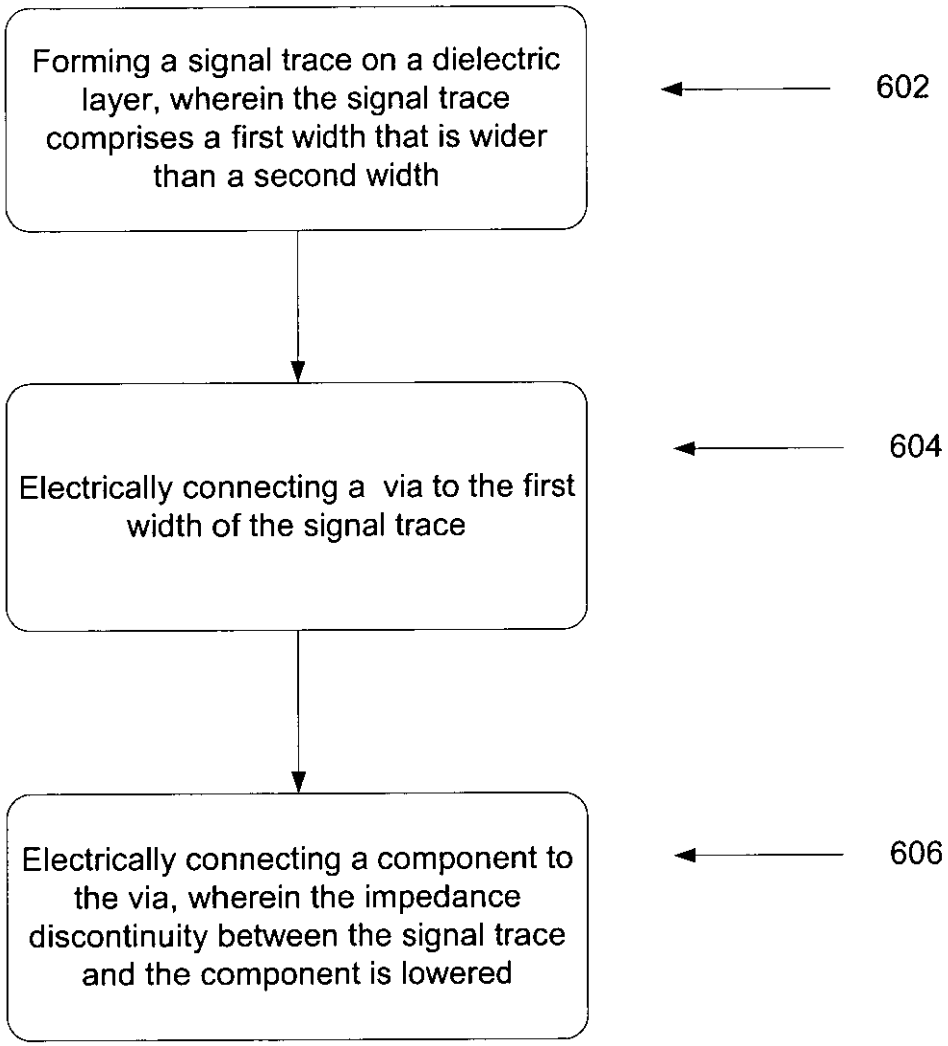
Forming a signal trace on a dielectric layer, wherein the signal trace comprises a first width that is wider than a second width
602
Electrically connecting a via to the first width of the signal trace
604
Electrically connecting a component to the via, wherein the impedance discontinuity between the signal trace and the component is lowered
606

FIG. 6